

A Low-power H.264 Codec LSI

July, 2008

Abstract

The latest video compression standard H.264, which is capable of achieving a compression ratio more than twice that of MPEG-2, has been widely spreading in the market of high-definition AV devices as a key technology of video coding. A developed low-power H.264 codec LSI achieves both high image quality and low-power at coding operation by using the original coding algorithm for high image quality and low-power codec architecture. This LSI is suitable for various application from portable AV products to professional-use equipments.

Technology

• High performance hardware engines for original coding algorithm

H.264 coding process generally requires over 10 times the complexity of MPEG-2. This LSI achieves a high image quality with with less computation, by using the following original coding algorithm based on the knowledge of Human Visual System (HVS) and optimum hardware engines which can execute the process with high performance by cooperating with internal CPU.

- A multi-stage motion estimation scheme with a fast decision-making algorithm which utilizes the characteristics of the block in previous picture and neighboring blocks in current pictures.
- A bit assignment algorithm which achieves stable visual quality by analyzing texture and movement of the input scene in the spatial and temporal domains.

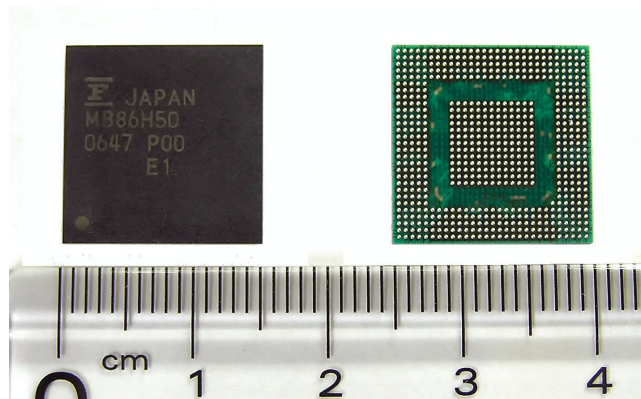
• Low-power codec architecture incorporating memory

In H.264 coding process of HDTV, one of the most difficulties in LSI design is high bandwidth and power consumption required for memory access between the codec chip and the external memory in which reference pictures are stored. This LSI, in which low power FCRAM is embedded, reduces the amount of memory access by using the following techniques and power consumption including memory required for H.264 coding process.

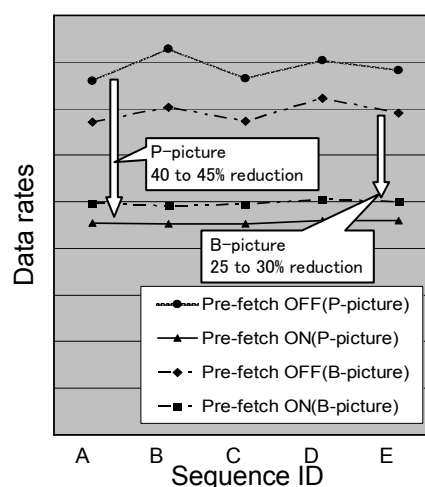
- Adaptive pre-fetch memory control according to the motion estimation process
- Reference block grouping technique which can reduce the amount of memory access at sub-block division

Application Examples

- Network equipment for HDTV transmission
- Portable AV products
- Hard disk recorders



H.264 codec LSI photograph



Data rates reduction by pre-fetch memory