

Power Integrity Analysis with LSI Noise Model

July, 2005

Abstract

Together with semiconductor technology scaling, power integrity inside digital consumer products has become a major design issue. As depicted in figure 1, power supply noise is generated by LSI operation, then propagates into PCBs, and finally radiates into the air as electromagnetic interference noise. All of this noise has a significant impact on electrical products. To investigate this, we created an LSI noise model and developed a simulation methodology to analyze power integrity. We also used this model in the initial design stage to optimize the power wiring, minimize the power pin count, and thereby minimize system costs. With this noise model, we can improve the quality of digital consumer products as well.

Technology

- The power supply line in LSI circuits consists of several billions of wirings. So the most difficult issue in generating the LSI noise model is compressing this many wirings and making a simpler model. We proposed a new model structure, called Power Unit model, and succeeded in compressing the size of the model to about one one-hundredth.
- We use this model to generate an initial design estimation method and design rules. We also incorporate this method and these rules into a Fujitsu LSI reference design flow.

Application Examples

- Figure 2 plots the results of power noise analysis. When many IO circuits switch simultaneously, power supply noise becomes very large. With our power integrity analysis, power supply noise distribution within an LSI can be easily analyzed.
- We applied this technique to the FR1000 embedded processor design. [IEEE International Solid-State Circuits Conference 2005 (10.7)]

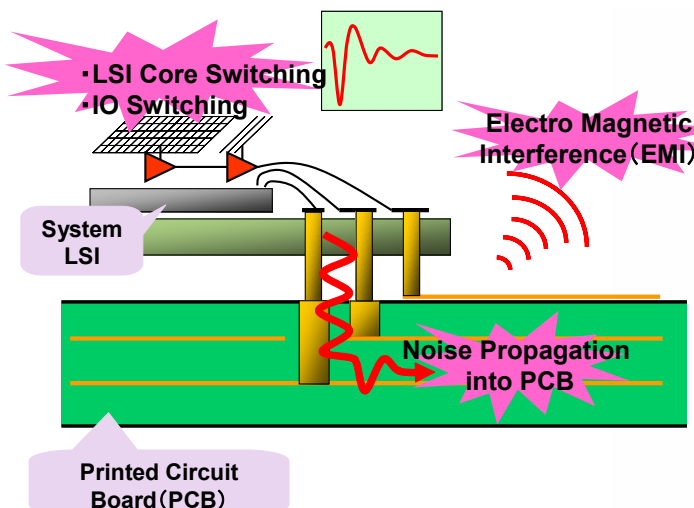


Figure 1. Behavior of Power Noise

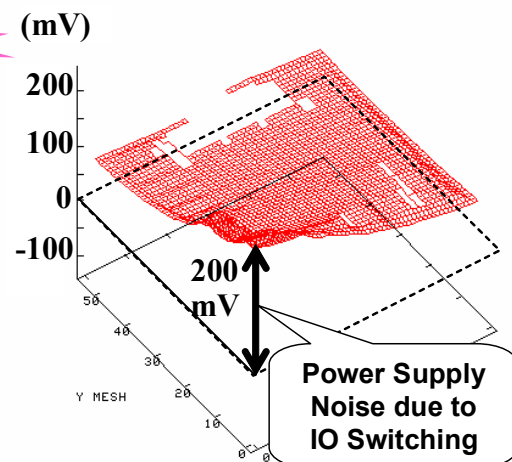


Figure 2. Result of Power Noise Analysis Inside a System LSI