

Pipelined A/D Converter

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Abstract

Now a days, demand for mobile communication systems operating longer time supplied from battery is increasing. In such background, low supply voltage tolerance as well as low power consumption are key issues, so that researching and developing for low power supply system on chip (SoC) are progressing. This means that A/D converter (ADC) is also required to operate in a low power supply, because ADC is usually implemented on the SoC.

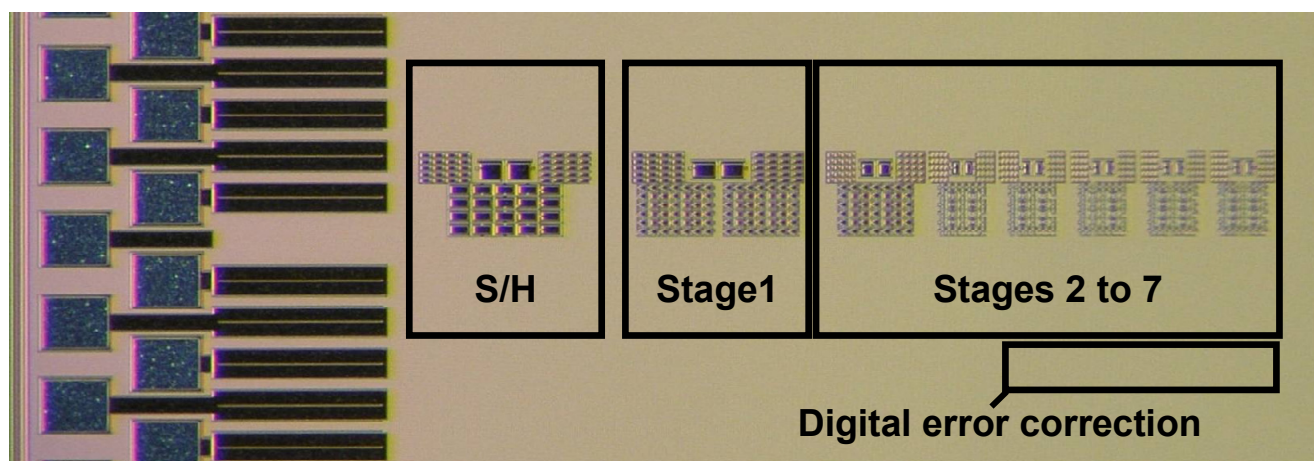
Fujitsu laboratories are investigating low power supply analog design for high performance pipelined ADCs. A low power design has been developed, which can maintain the performance down to 0.8V supply voltage by a robust biasing technique.

Technology

One of the fundamental issues for analog design is that maintaining MOS FETs to work in saturation region. A biasing technique is developed to maintain the overdrive voltages constant in all conditions, process distribution, power supply and temperature which need for robust operation. The design has been implemented in the actual pipelined ADC, 10-bit 80MS/s in 90nm CMOS technology, keeping the performance down to 0.8V power supply with 6.5mW power consumption. This result has been published at IEEE International Solid-State Circuits Conference 2007.

Application Examples

Communication systems such as digital television tuner and WiMAX, contributing to improve the energy efficiency.



10b 80MS/s Pipelined ADC