

Low-Power, High-Performance 45nm Logic Chips

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Abstract

We have developed a platform technology for 45nm generation LSI logic chips, which combines technologies for low power consumption and high-performance interconnect. Compared to previous 45nm technologies on record, the new platform reduces the leakage current that occurs when current is wasted in wait states to one-fifth that of previous levels and reduces interconnect-induced lag times by approximately 14%. The realization of these new 45nm generation platform technologies will enable Fujitsu Microelectronics to offer its customers LSI logic chips that feature even higher speeds, smaller size and lower power consumption than currently available.

Technology

• New annealing technology

We found that forming shallower source and drain regions is an effective way to reduce leakage current (Figure 1). However, simply making them shallower also increases resistance at the source and drain regions, thereby degrading transistor performance. To counteract this, we developed a new annealing technology called millisecond annealing (MSA). Compared to previous annealing, our millisecond annealing technology uses higher temperatures thus enabling reduction of resistance, and because the annealing time is brief it is possible to form shallow source and drain regions and thereby reduce leakage current.

• High-performance interconnects

We used nano-clustering silica (NCS), which has a dielectric constant (k) of 2.25 - the lowest of any insulating film reported to date - in a lower interconnect region suitable for the smallest interconnect spaces (Figure 2). NCS is an insulating material pocked with miniscule holes, enabling both a low dielectric value and high mechanical strength simultaneously. We introduced NCS on a partial basis beginning with the 65nm generation. However, for the 45nm generation, NCS not just within a given interconnect layer but also between different layers to further reduce interconnect capacitance.

Application Examples

These two newly developed technologies enable the reduction of leakage current during standby, while simultaneously increasing operating speed. Fujitsu Microelectronics incorporates these technologies into LSIs that are suited for mobile devices as part of a ubiquitous networking society.

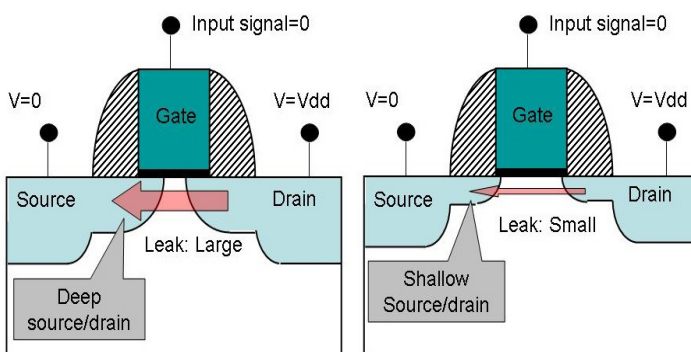


Figure 1. Relation between source/drain junction depth and leak current

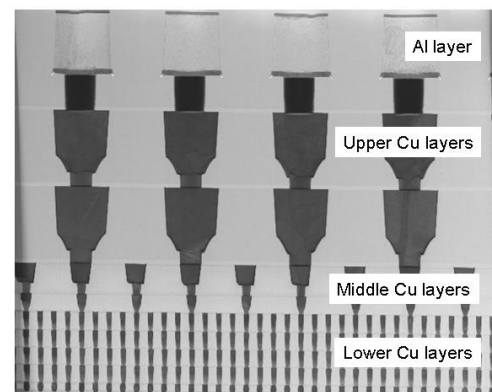


Figure 2. Cross-section of 9Cu + 1Al interconnect module with Full-NCS at lower Cu layers